Examination (SS 2019)
Communication Systems and Protocols

Institut für Technik der Informationsverarbeitung
Prof. Dr.-Ing. Dr. h. c. Jürgen Becker
Dr.-Ing. Jens Becker

Exam: Communication Systems and Protocols
Date: September 20, 2019

Participant:
Matr. №:
ID:

Lecure hall:
Seat №:

The following rules apply:

- The writing time of the examination is 120 minutes.
- No examination aids are permitted, except for
  - one double-sided DIN-A4 sheet of hand-written notes,
  - a non-programmable calculator and
  - a dictionary.
- Use **permanent ink** only. The usage of pencils or red color is prohibited.
- You are not permitted to use your own writing paper.
- Please do not write on the back sides of the sheets.
- Additional solution sheets are available from the examination supervisors.
  - Make sure that you label all such sheets with your matriculation number.
  - Each additional solution sheet needs to be assigned to exactly one task.

The examination comprises **37 sheets**.

Task 1: Physical Basics

35

Task 1.1: Differential Signaling

A) Name two advantages of differential signal transmission over single-ended signaling.

2

1pt per item.

- Electric potential between signal lines is doubled -> longer distances or smaller voltage levels possible.
- Inherent compensation of disturbances: A noise pulse affects both lines and therefore is not visible in the differential signal.

B) For the following schematic of an Emitter Coupled Logic (ECL) sender compare the case when Input is HIGH ($Input_H$) and when Input is LOW ($Input_L$). Consider the currents I_{T_1} ... I_{T_4} flowing through the transistors T_1 ... T_4 and the output voltages V_{Out_1} and V_{Out_2}. In the boxes indicate if these currents and voltages, respectively, are higher (>), lower (<) or equal (=) for $Input_H$ in comparison to $Input_L$.

6

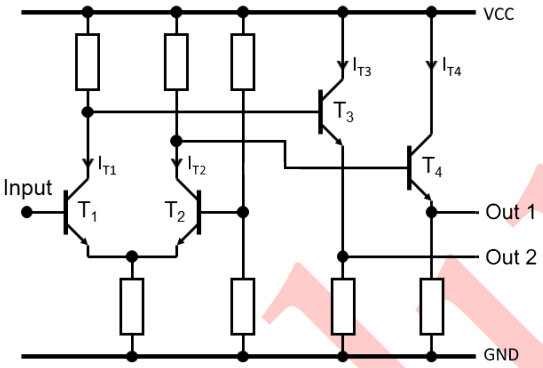


Figure 1.1: Diffential output driver

1pt per line

$I_{T_1}(Input_H)$	>	$I_{T_1}(Input_L)$
$I_{T_2}(Input_H)$	<	$I_{T_2}(Input_L)$
$I_{T_3}(Input_H)$	<	$I_{T_3}(Input_L)$
$I_{T_4}(Input_H)$	>	$I_{T_4}(Input_L)$
$V_{Out1}(Input_H)$	>	$V_{Out1}(Input_L)$
$V_{Out2}(Input_H)$	<	$V_{Out2}(Input_L)$

Task 1.2: Communication Buses

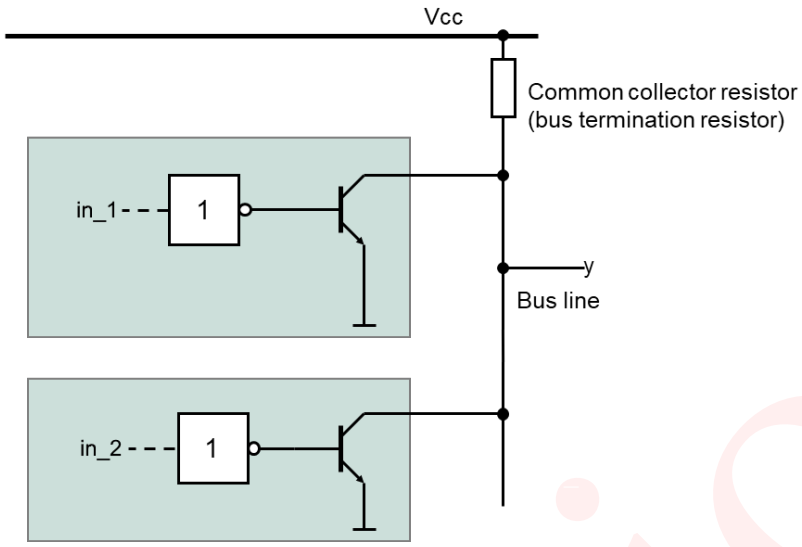
A) Name two ways to avoid short circuits when connecting multiple senders to a bus line.

2

1pt per item

- Use tristate drivers
- Use open collector drivers

B) Draw a bus line with two open-collector drivers. The drawing should make clear how the nodes pull the line to VCC and/or GND level. Indicate the node input lines by in_1 and in_2 and the bus line by y. The bus voltage level shall be equal to the node's input voltage level (when sending the dominant level). **5**



+2pt for basic structure (separate voltage (i.e. V_{CC}), pull-up resistor, 2 transistors).
+2pt for added inverters.
+1pt for correct labelling ($in_{1,2}$, y).

C) Explain the concept of "Wired AND" in bus communications. **2**

If the drivers in combination with the bus line implement an AND function, this is called "Wired AND". In this case, '1' will be read if all nodes transmit '1' while '0' will be received if at least one node transmits a '0'. **2pt if correct**

Task 1.3: Reflection on wires

A) A long signal line can be modelled as a sequence of quadripoles each representing an infinitesimally short segment of the line. Explain the four components R', L', C', and G' and what they represent in this model. **4**

1pt per item

- series resistance R' representing the resistance of the conductors
- series inductance L' representing the inductance caused by the magnetic field around the wires
- parallel capacitance C' representing the capacitance between the conductors
- parallel conductance G' representing the conductance (of the dielectricum) between the conductors

B) Which components of the quadripole model are known in the lossless case? Give the values for these components. **2**

$R' = 0, G' = 0$

2pt if correct (consider naming convention defined in previous task)

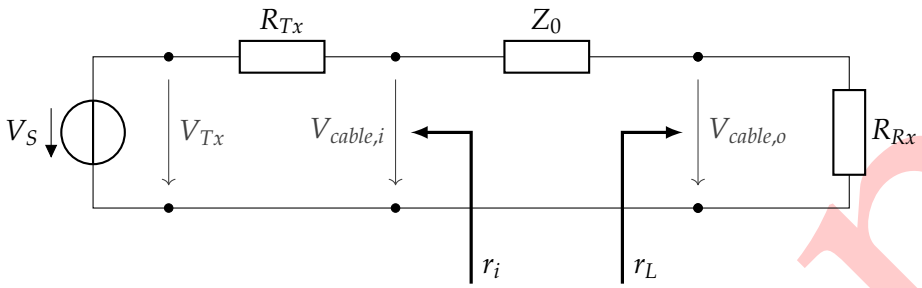


Figure 1.2: Test setup

In Figure 1.2, the equivalent circuit diagram of an ideal (lossless) transmission line is depicted. A transmitter having output impedance R_{Tx} is connected to a receiver with the input impedance R_{Rx} using a long cable.
The signal line is characterized by $Z_0 = 30\,\Omega$. $R_{Tx} = 50\,\Omega$, $R_{Rx} = 90\,\Omega$.

C) Give the formula for calculating the reflection factors in general. Give the value of the reflection factors r_i and r_L. **3**

$r = (R_T - Z_0)/(R_T + Z_0)$
$r_i = (R_{Tx} - Z_0)/(R_{Tx} + Z_0) = \frac{1}{4} = 0.25$
$r_L = (R_{Rx} - Z_0)/(R_{Rx} + Z_0) = \frac{1}{2} = 0.5$

1pt for abstract formular (a more general formula is also accepted)
1pt each for correct r_i and r_L value (formula not needed)

At the time $t = 0$ the voltage V_S of the sender changes from 0 V to 16 V and is constant afterwards. The run time of a wave on the cable is t_d.

D) Calculate the value of the voltage $V_{cable,i}$ at the time $t = 0$. **3**

At the time $t = 0$ the wave only „sees“ a series connection of the internal resistance R_{Tx} and the wave impedance Z_0.

2pt for correct apoproach and formula
1pt for correct value

$$V_{cable,i}(0) = V_S \cdot \frac{Z_0}{R_{Tx}+Z_0} = 16\,\text{V} \cdot \frac{30\,\Omega}{50\,\Omega+30\,\Omega} = 6\,\text{V}$$

E) Calculate the voltage $V_{cable,m}$ in the middle of the line at the times $t \in \{0, t_d, 2t_d, 3t_d\}$. Neglect all transient events, use ideal rectangular impulses for calculation. **4**

1pt per time step

$V_{cable,m}(0t_d) = 0\,\text{V}$ (since the wave has not reached this point yet).
$V_{cable,m}(1t_d) = 6\,\text{V}$ (see previous task).
$V_{cable,m}(2t_d) = V_{cable,m}(1t_d) + r_L \cdot [V_{cable,m}(1t_d) - V_{cable,m}(0t_d)] = 9\,\text{V}$
$V_{cable,m}(3t_d) = V_{cable,m}(2t_d) + r_i \cdot [V_{cable,m}(2t_d) - V_{cable,m}(1t_d)] = 9.75\,\text{V}$
Not needed:
$V_{cable,m}(4t_d) = V_{cable,m}(3t_d) + r_L \cdot [V_{cable,m}(3t_d) - V_{cable,m}(2t_d)] = 10.125\,\text{V}$

F) What needs to be fulfilled to avoid reflection at the end of the line? Give the general requirement. What can be done to achieve this for the receiving side of the setup shown in Figure 1.2 (no calculation required)?

2

1pt for termination criteria (formula or explanation)
1pt for a solution

The line impedance must equal the termination resistance.

Option 1: Parallel resistor for termination
Since $R_{Rx} > Z_0$, a parallel resistor R_x needs to be added so that $Z_0 = R_{Rx} \parallel R_x$.

$$Z_0 = R_{Rx} \parallel R_x$$
$$\frac{1}{Z_0} = \frac{1}{R_{Rx}} + \frac{1}{R_x}$$
$$\frac{1}{R_x} = \frac{1}{Z_0} - \frac{1}{R_{Rx}}$$
$$R_x = \frac{1}{\frac{1}{Z_0} - \frac{1}{R_{Rx}}} = \frac{1}{\frac{1}{30\,\Omega} - \frac{1}{90\,\Omega}} = 45\,\Omega$$

Option 2: replace receiver with a component having $R_{Rx} = Z_0$.

Option 3: replace the cable so that $Z_0 = R_{Rx}$.

Task 2: Transmission Principles

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Task 2.1: Line Codes

5

A) We want to transmit the value "1001 0110 0111" through a serial wire communication channel. Complete Figure 2.1 with the digital signals transmitted using each given encoding scheme.

1p for each correct line code

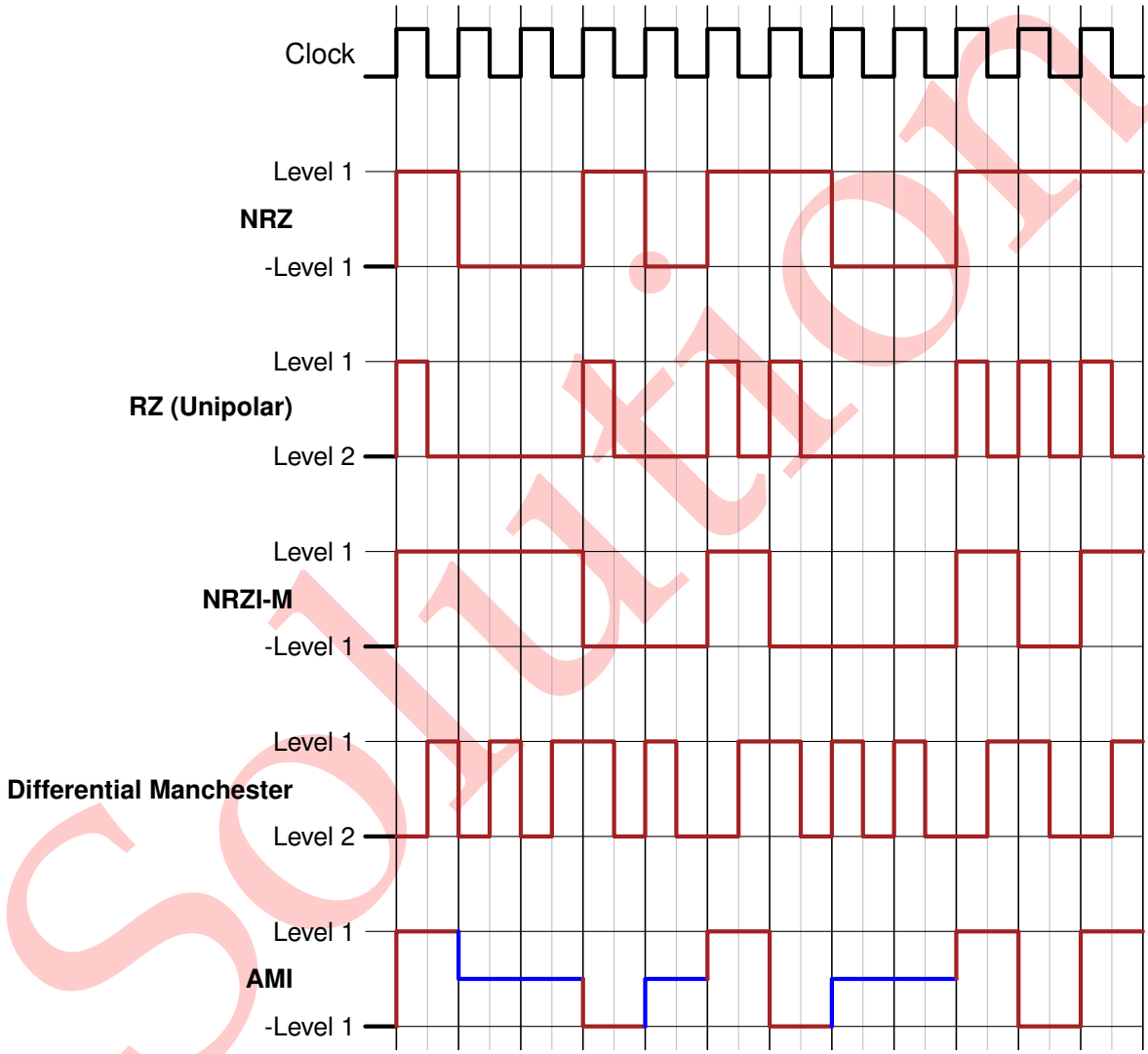


Figure 2.1: Line codes

B) Classify the line codes given in Question A according to their clock recovery properties. Do the codes always have this property? Justify your answer for each of the codes. **5**

1pt. for each code, if the property is correct and with justification.

NRZ: no, clock recovery not possible or no clock recovery mechanism

Unipolar RZ: no, impossible to recover timing information for long sequences of 0's

NRZI-M: no, clock recovery not always possible, if long sequences of 0's

Differential Manchester: yes, since at least one signal transition occurs per bit interval

AMI: no, if there are long '0'-sequences

C) An approach used to synchronize communication processes is the use of Flow-Control. Complete the signals in figure 2.2 to perform two transmissions of DATA values 0xA and 0x5 using Level-Triggered Closed-Loop Flow Control II. This approach uses Valid and Busy signals. A grey color symbolises that the DATA line is idle and that no value is being driven on the bus. Ignore delays and consider that a read occurs at the rising edge and signal change at falling edge of the clock, and that the receiver required 1 cycle to read the value. **6**

1p for each correct transition in each clock edge:
- VALID and DATA (0xA for first transmission and 0x2 for second)
- BUSY assertfor 1 cycle after VALID=1
- VALID and DATA deassert after BUSY=0

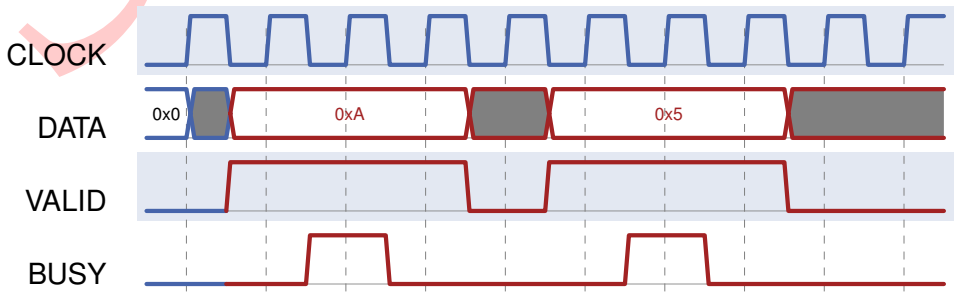
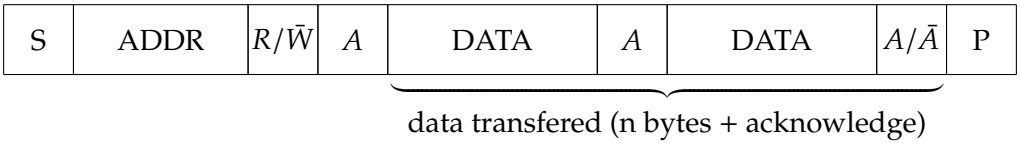


Figure 2.2: Signal sequence

Task 2.2: I²C Communication

In this task we want to investigate the data transmission on the I²C-Bus. The simplified frame format is given in Figure 2.3. Three master nodes are simultaneously trying to transmit or read one byte of data to or from different slaves over the I²C-Bus.



term	descripion
S	start condition
ADDR	7-bit slave address
$R/\bar{W}$	read/write: read 1, write 0
A	acknowledge ('0')
$\bar{A}$	not acknowledge ('1')
DATA	8-bit data
P	stop Condition

Figure 2.3: I²C-Bus frame format

A) Is I²C a synchronous or asynchronous protocol? Justify your answer. **2**

It is a Synchronous Protocol because it sends the transmitter's clock through SCL. **2p for SCL/presence of clock line**

B) Consider the following cases where two masters try to access the same slave. **6**
Case 1: Two masters try to perform a read operation at the exact same time.
Case 2: Two masters try to perform a write operation at the exact same time.
Case 3: One master tries to read and the other master tries to write at the exact same time.
What happens in each case ? Is the write or read operation successful in each case? Explain if any collisions could be detected and how they are detected. Justify your answer for each of the cases.

If both Masters try to read, they both receive the same data from the Slave and no collision is detected.
If both try to write, the Master who writes the smallest value (first to write a '0') gets priority and completes the operation, a collision is detected during the writing of the data.
If they ask for different operations, the write operation has priority as it correspond to a '0' bit, and a collision is detected before the data is sent.

2p for each case with explanation.

C) The diagram in Figure 2.4 corresponds to a I^{2}C Multimaster configuration. The system is composed of 3 Slave and 3 Master nodes. Complete the diagram with the signals generated by each node for the simultaneous transactions presented in Table 2.1 and for the resulting SDA line of this bus. The table shows for each master, the address of the slave it is accessing, the communication mode (R/W) and the data to be sent or read. **8**

2p for correct SDA line.
1p for correct address and R/W request for each Master (3p total for all 3).
1p for correct assignment of all A/not A by Slaves.
1p for correct assignment of Stop Condition.
1p for correct data of Slaves

node	slave address	R/$\overline{W}$	data
Master 1	1011101	0	01111001
Master 2	1010101	1	01011010
Master 3	1010111	0	01000011

Table 2.1: I^{2}C Communication Parameters

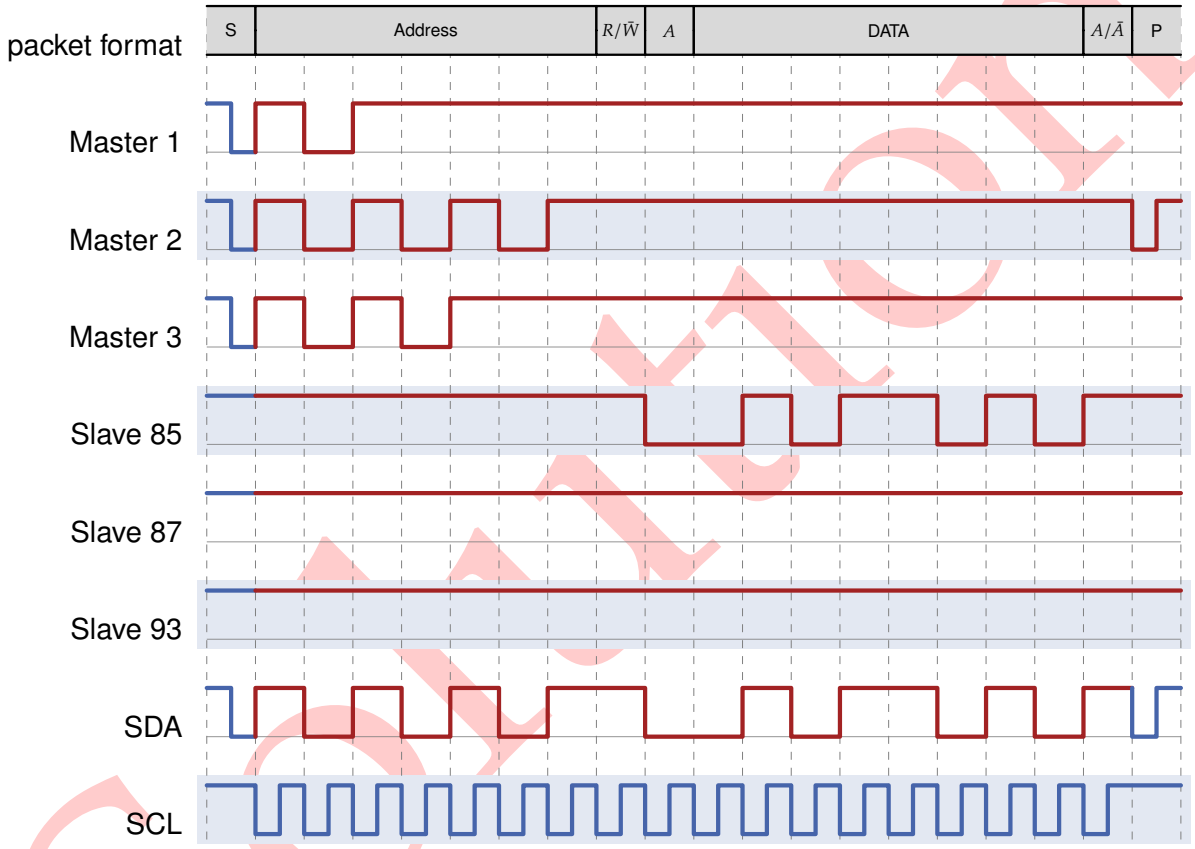


Figure 2.4: I^{2}C Signal sequence

Task 3: Modulation and Spread Spectrum

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Task 3.1: Modulation

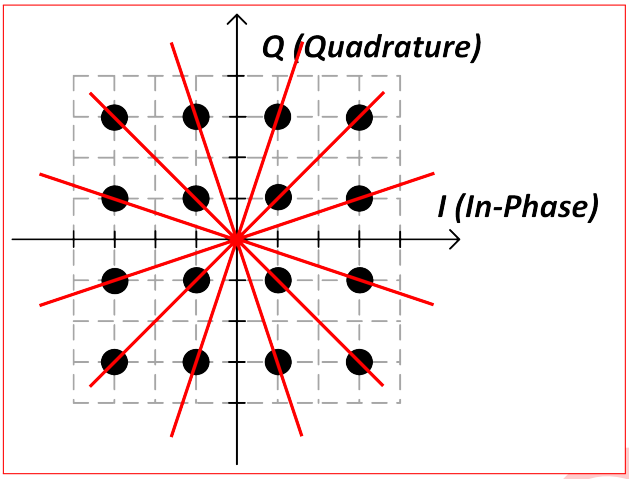


Figure 3.1: Constellation Diagram

A) The constellation diagram of a certain modulation scheme is shown in Figure 3.1. How many possible phase values can be used in this modulation scheme? Indicate the values in the Figure 3.1.

3

12 values (12 different angles)

1pt for mentioning twelve values and 2 pt for sketching values in the figure.
-1pt for each incorrect sketch, min 0pt for sketch

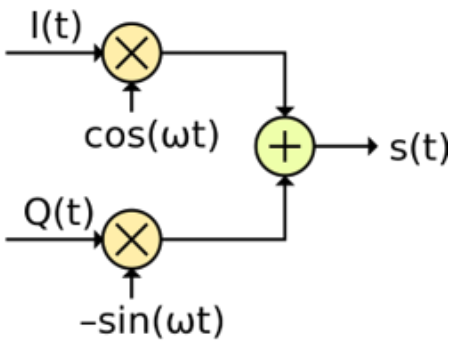
B) How many carrier frequencies are used in the QAM modulation scheme?

1

QAM uses one carrier frequency

C) Draw a block diagram (using adders and multipliers) for the QAM modulator. Use $I(t)$ and $Q(t)$ as names for the inputs and $s(t)$ as name for the output.

3



2*mult with carrier: 1pt, 90 deg phase diff: 1pt, addition: 1pt, sign doesn't matter

12

D) A constellation diagram of an 8-QAM scheme is shown in Figure 3.2. The bits **111001110100** shall be transmitted and will be encoded from the left to the right. The Figure 3.3 shows the in-phase carrier signal (B), in-phase symbol (A), and in-phase modulated signal (C). Figure 3.4 shows the quadrature carrier signal (E), quadrature symbol (D), quadrature modulated signal (F). Use Figure 3.3 (A and C) and Figure 3.4 (D and F) to sketch the waveforms of symbol representations and modulated information signals seen from in-phase and quadrature axes. The symbol period is twice as long as the period of carrier signal.

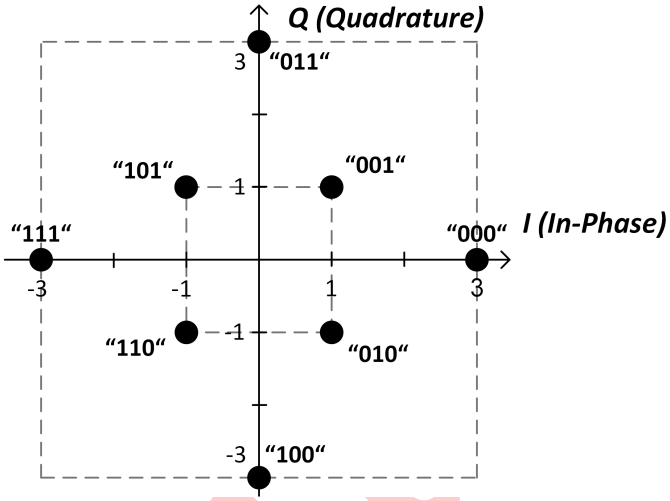
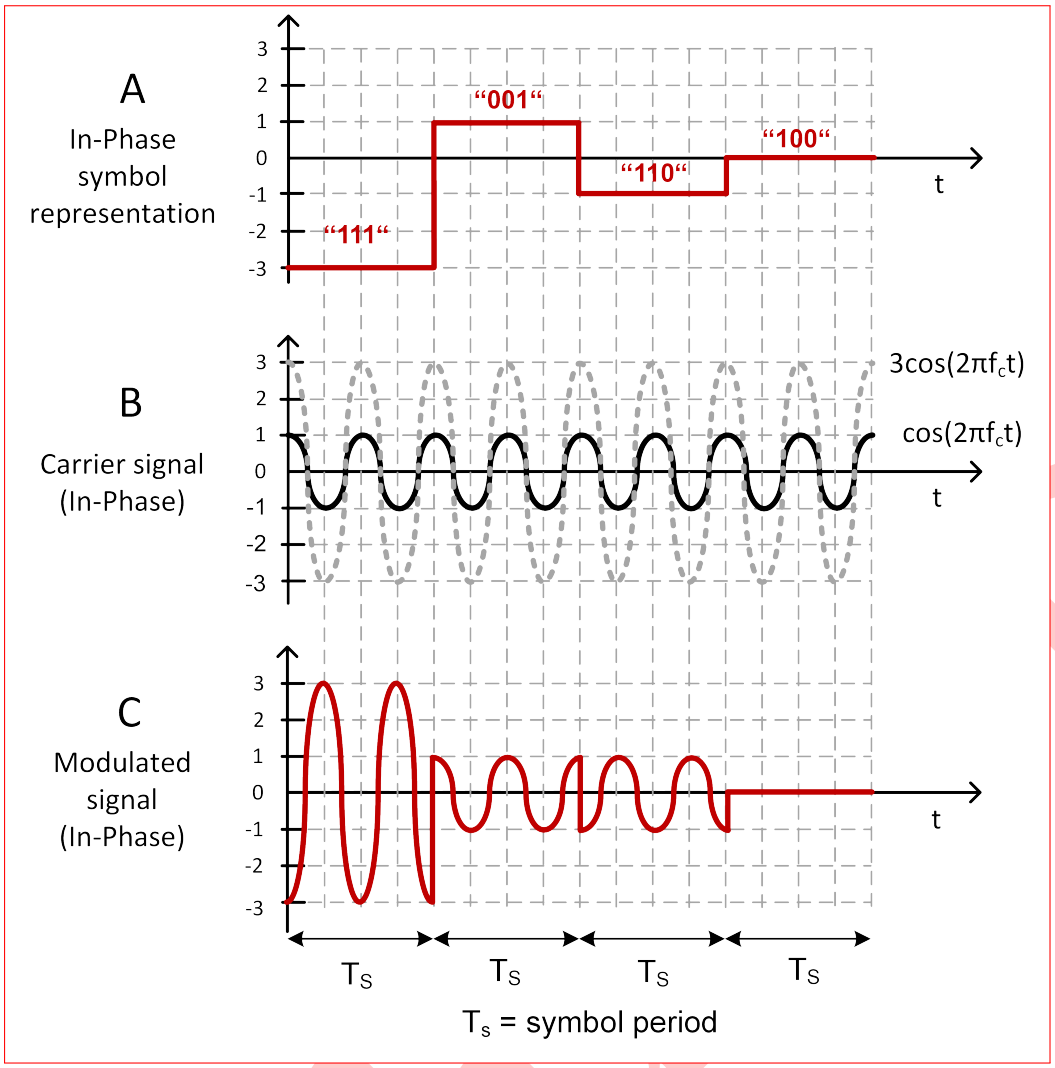


Figure 3.2: Constellation Diagram of an 8-QAM scheme



Instructions apply to both Figure 3.3 and Figure 3.4.

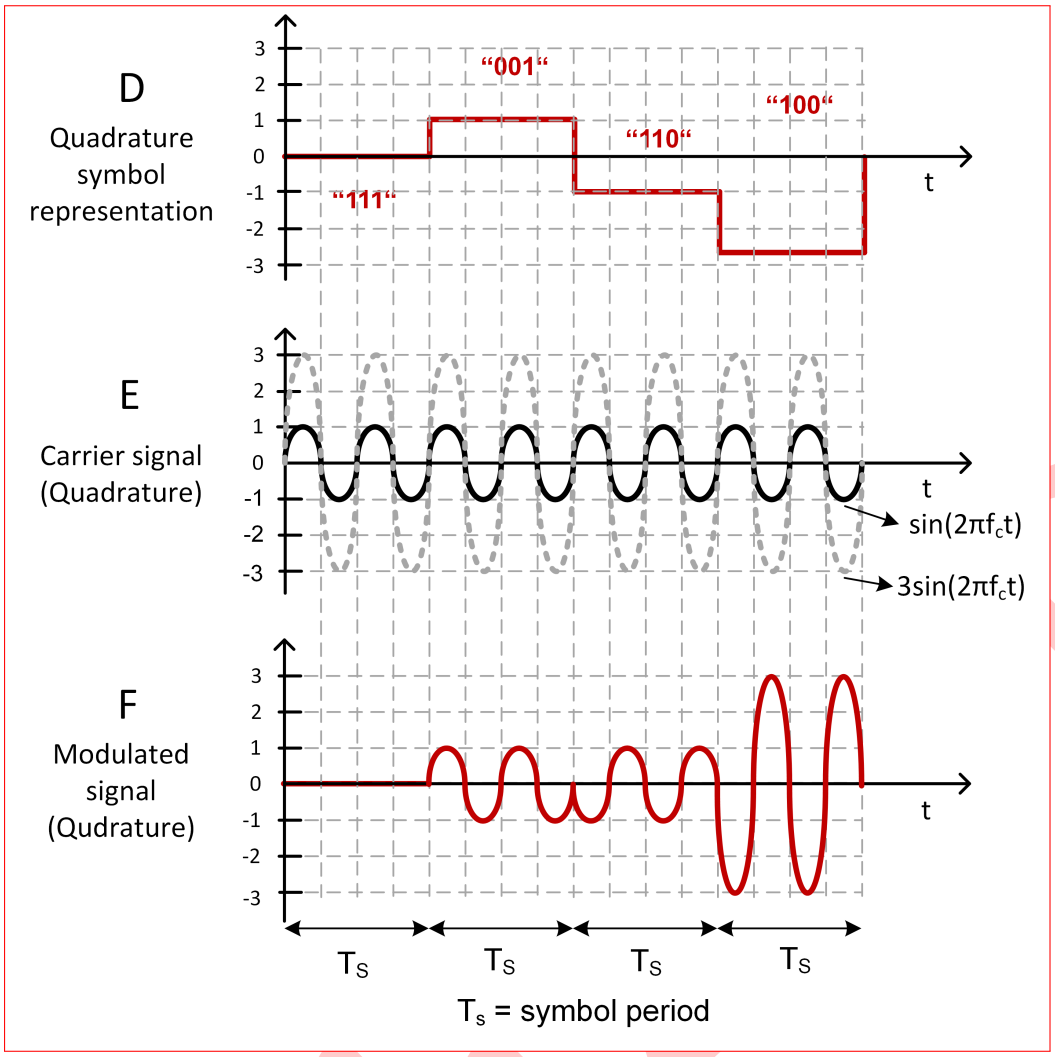
2pt if A is correct.

2pt if Amplitude in C matches A

2pt if Phase in C matches A

No points for C if A has less than 3 different levels.

Figure 3.3: In-Phase Symbol Representation, Carrier Signal (In-Phase), and Modulated Signal (In-Phase)



As in Figure 3.3.

Figure 3.4: Quadrature Symbol Representation, Carrier Signal (Quadrature), and Modulated Signal (Quadrature)

Task 3.2: Spread Spectrum

5

A) The Walsh functions in Table 3.1 shall be used for the simultaneous transmission of eight nodes. To determine which signal is sent, complete the blank cells in the *Signal to be Sent* column of Table 3.2 for each node.

5P for correct Signal to be Sent for all nodes
-1P per wrong Signal.

Sender Node	Function							
0	+1	+1	+1	+1	+1	+1	+1	+1
1	+1	-1	+1	-1	+1	-1	+1	-1
2	+1	+1	-1	-1	+1	+1	-1	-1
3	+1	-1	-1	+1	+1	-1	-1	+1
4	+1	+1	+1	+1	-1	-1	-1	-1
5	+1	-1	+1	-1	-1	+1	-1	+1
6	+1	+1	-1	-1	-1	-1	+1	+1
7	+1	-1	-1	+1	-1	+1	+1	-1

Table 3.1: Walsh Functions for Nodes

Node	Data	Signal to be Sent							
0	"0"	-1	-1	-1	-1	-1	-1	-1	-1
4	"0"	-1	-1	-1	-1	+1	+1	+1	+1
5	"0"	-1	+1	-1	+1	+1	-1	+1	-1
6	"1"	+1	+1	-1	-1	-1	-1	+1	+1
others	"silent"	0	0	0	0	0	0	0	0
Signal on Media		-2	0	-4	-2	0	-2	+2	0

Table 3.2: Transmission with CDMA

B) In the *Signal on Media* row of Table 3.2, write down the summation value when nodes 0,4,5,6 are sending data as shown and other nodes are silent. Now consider a case where one node connected to the bus wants to receive the data encoded by node 4. Write down the summation value which would be calculated by the receiver node. Explain how you calculate the received value and write down the calculation steps.

3

Calculate the inner product of the sent value with the Walsh code of the node we want to receive from.
$n_4 = (-2, 0, -4, -2, 0, -2, +2, 0) \cdot (+1, +1, +1, +1, -1, -1, -1, -1) = -8$

2P for Signal on Media and 1P for summation correct answer

C) Consider a case where one node connected to the bus wants to receive data sent by node 1. Use the *Signal on Media* values computed in the previous task and write down the summation value which would be calculated by the receiver node. Write down the calculation steps. Consider that there is no disturbance in the bus.

1

$n_1 = (-2, 0, -4, -2, 0, -2, +2, 0) \cdot (+1, -1, +1, -1, +1, -1, +1, -1) = 0$

1p for correct answer

D) Show that Walsh function 0 is orthogonal to function 1. Also give the result of the inner product of Walsh function 0 with itself.

2

2p total -1 per mistake

$n_0 \cdot n_1 = (1, 1, 1, 1, 1, 1, 1, 1) \cdot (1, -1, 1, -1, 1, -1, 1, -1) = 0$
$n_0 \cdot n_0 = (1, 1, 1, 1, 1, 1, 1, 1) \cdot (1, 1, 1, 1, 1, 1, 1, 1) = 8$

E) Explain why the orthogonality is required for this CDMA scheme.

1

The orthogonality ensures the inner product of the send data contributed by different nodes is zero for all nodes, except for the one we want to receive from. The functions do not interfere with each other

Accept most solutions

Task 4: Media Access

28

Task 4.1: CSMA/CD

Ethernet is a family of computer networking technologies commonly used in local area networks (LANs) and metropolitan area networks (MANs). Systems communicating over Ethernet divide a stream of data into shorter pieces called frames. Each frame contains source and destination addresses, and error-checking data so that damaged frames can be detected and discarded. The "Carrier Sense Multiple Access with Collision Detection" scheme is used to control access to the shared medium.

A bus system with several nodes is using an Ethernet standard with a transmission rate of 10 Mbit/s and a signal speed of $2 \cdot 10^8$ m/s. A maximum distance of 1.5 km for two nodes has to be considered.

A) Two nodes n_1 and n_2 want to send data at the same time and the shared media is not occupied at this moment. Describe the sending procedure and necessary actions of node n_1 until the transmission is fully completed.

6

Node n_1 checks the shared media and starts sending data (also node n_2), there will be a collision on the shared media. Both nodes are always reading the channel and check if the signal sent is identical to the one being read and detects collision. Both senders will detect a collsion and will send a JAM signal and transmission is ceased. After an induvidual delay time the senders will try to send the data again.

1pt for direct sending(medium is free)
1pt for reading channel
1pt for collision detection
1pt for JAM signal
1pt delay time
1pt sending again

B) Why is it necessary to establish minimal packet length when using CSMA/CD as arbitration scheme?

2

A minimal packet length is necessary to detect a collision.

2pt for collision detection

C) Calculate the resulting minimal package length in bits for the bus system.

4

minimal time on the line for one package: $t = \frac{2 \cdot l}{v} = \frac{2 \cdot 1.5\,\text{km}}{2 \cdot 10^8\,\text{m/s}} = 1.5 \cdot 10^{-5}\,\text{s}$
minimal package length: $PL \geq t \cdot TR = 1.5 \cdot 10^{-5}\,\text{s} \cdot 10\,\text{Mbit/s} = 150\,\text{bit}$

2pt for 2 times the length
2pt for correct amount of bits

D) A minimal package length of 64 bytes for the bus system is chosen. The bus system is illustrated in Figure 4.1 and is used with a transmission rate of 10 Mbit/s and a signal speed of $2 \cdot 10^8$ m/s. Each repeater will add a delay of four bits. Is this bus system working with these constraints? Give an explanation!

6

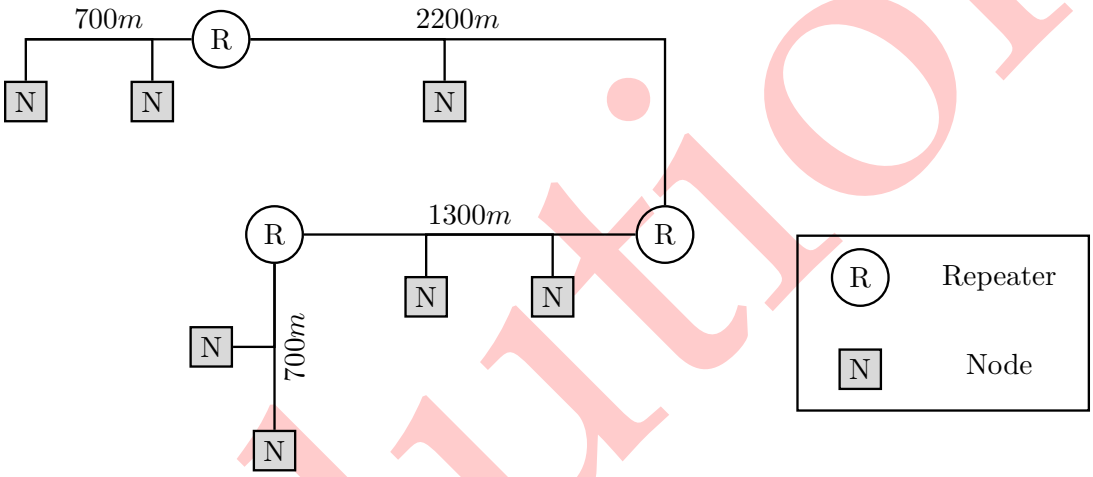


Figure 4.1: Ethernet topology

$PL \geq t \cdot TR = \frac{2l}{v} \cdot TR \Leftrightarrow l \leq \frac{PL \cdot v}{2 \cdot TR}$

$\Rightarrow l \leq \frac{PL \cdot 2 \cdot 10^8\,\text{m/s}}{2 \cdot 10\,\text{Mbit/s}} = 10\,\text{m/bit} \cdot PL$

A delay of 3*4*2 bits has to be considered.

$\Rightarrow l + l_{delay} \leq 10\,\text{m/bit} \cdot PL$
with $l_{delay} = \frac{24\,\text{bit} \cdot v}{TR} = 480\,\text{m}$ and $l = 4900\,\text{m}$

$\Rightarrow 4900\,\text{m} + 480\,\text{m} \leq 10\,\text{m/bit} \cdot PL$ with $PL = 512\,\text{bit}$
$\Rightarrow 5380\,\text{m} \leq 5120\,\text{m}$
$\Rightarrow$ A secure detection of collisions is not possible

2pt for correct ansatz
2pt for correct delay
2pt for correct solution

Task 4.2: CSMA/CR

A bus system of four nodes is using CSMA/CR as arbitration scheme and is connected via open collector drivers and a wired-AND connection. Each node has a five Bit identifier and the bus has to cover a maximum distance of 600m.

A) Name two advantages of CSMA/CR in contrast to CSMA/CD, explain your answers briefly. **4**

no data destruction (arbitration phase), better channel utilization (no collisions), (very limited) real time capability (prioritisation by IDs)

2pt for correct answer (only with explanation)

B) The data format includes a frame with a Start Of Frame bit (SOF) and an identifier with five bits. The identifiers can be taken from Table 4.1. Using Figure 4.2, draw the impulse **6**

Node	Identifier
A	10101
B	10011
C	10010
D	10100

Table 4.1: Identifiers of the nodes

diagram for the arbitration of the single nodes and the signal level of the shared bus line. Which node is granted exclusive access to the bus?

Node C is granted exclusive access to the bus.

1p for correct dominant SOF
1p for each consecutive correct time step (max 4P)
1p for correct winning node and last time step

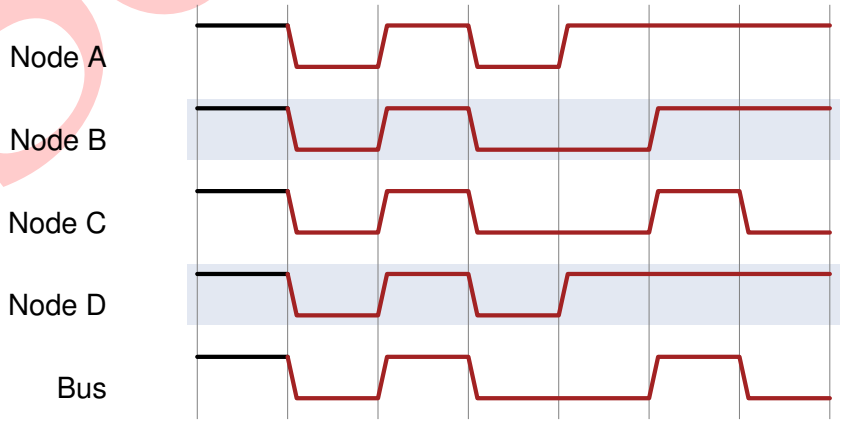


Figure 4.2: Bus Access

Task 5: Error Protection

30

Task 5.1: Cyclic Redundancy Check (CRC)

A) Given a CRC generator polynomial of $G(x) = x^5 + x^4 + 1$, what is the maximum burst error length that is guaranteed to be detectable in a CRC-protected frame? Justify your answer.

2

$G(x)$ has a degree of five. This means that in a data frame that comprises a CRC checksum based on $G(x)$, burst errors with a length ≤ 5 can always be detected.

+2 p. for the correct answer (reason and numeric value).

B) Assume that a specific CRC scheme employs $G(x) = x^4 + x^3 + x^2 + 1$ as its generator polynomial. Does this guarantee the detection of all error patterns with an odd number of erroneous bits in a protected frame? Justify your answer.

3

If $G(x)$ contains $(x + 1)$ as a factor, the detection of all error patterns with an odd number of erroneous bits is guaranteed. This sufficient condition is fulfilled:

+1 p. for the statement that $G(x)$ being divisible by $(x + 1)$ is a sufficient condition for this.

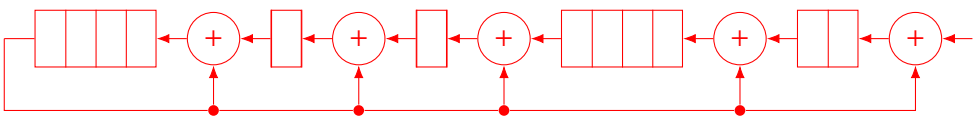
+2 p. for the polynomial division and the correct conclusion.

```
1 1 1 0 1 : 1 1
1 1
-------
0 0 1 0
    1 1
    -----
    0 1 1
      1 1
      -----
      0 0   ⇐ Remainder
```

Therefore, this CRC scheme is able detect all of the described error patterns.

C) Draw the simplified form of the linear feedback shift register with XOR operations implementing the CRC generator polynomial $G(x) = x^{12} + x^8 + x^7 + x^6 + x^2 + 1$.

3



3 p. if everything is correct.
2 p. if there is one mistake.

D) Assume that the message "1101 0100 1110" is to be transmitted over a channel. In order to enable the receiver to detect transmission errors, a CRC checksum based on the generator polynomial $G(x) = x^6 + x^3 + x^2 + x + 1$ shall be added. Calculate the corresponding checksum and give the bit string that is sent to the receiver.

7

```
1 1 0 1   0 1 0 0   1 1 1 0   0 0 0 0   0 0  :  1 0 0 1 1 1 1
1 0 0 1   1 1 1
-------------------------------------------------------------
  1 0 0   1 0 1 0
  1 0 0   1 1 1 1
-------------------------------------------------------------
  0 0 0   0 1 0 1   1 1 1 0
            1 0 0   1 1 1 1
-------------------------------------------------------------
            0 0 1   0 0 0 1   0 0
                1   0 0 1 1   1 1
-------------------------------------------------------------
                0   0 0 1 0   1 1 0 0   0
                        1 0   0 1 1 1   1
-------------------------------------------------------------
                        0 0   1 0 1 1   1 0
```

Starting from 6 p. for the correct calculation, -2 p. for a simple calculation error. No points if a systematic error was made.

If no systematic error was made: +1 p. for the correctly given bit string.

The checksum "101110" is appended to the given message. Therefore, the transmitted bit string is given as "1101 0100 1110 1011 10".

E) Suppose that for CRC protection, a sender and a receiver have agreed upon the generator polynomial $G(x) = x^5 + x^2 + x + 1$. Perform the CRC error detection scheme that the receiver carries out for the received bit string "0110 1000 0011 1". Which guarantee can the receiver deduce from the result with respect to single-bit errors?

4

```
0 1 1 0   1 0 0 0   0 0 1 1   1  :  1 0 0 1 1 1
  1 0 0   1 1 1
-----------------------------------------------
  0 1 0   0 1 1 0
    1 0   0 1 1 1
-----------------------------------------------
    0 0   0 0 0 1
                1   0 0 1 1   1
-----------------------------------------------
                0   0 0 0 0   0
```

+2 p. for the correct calculation. No points if a calculation or a systematic error was made.

If no systematic error was made: +2 p. for the correct conclusion.

The receiver calculates a remainder of zero and is therefore unable to detect an error. Since every single-bit error is detectable, the receiver obtains the guarantee that no single-bit error has occurred.

Task 5.2: Controller Area Network (CAN)

5

A) Consider a CAN network that consists of three individual CAN nodes. Suppose that one of these nodes, in the following referred to as the sender, transmits a data frame that is received by the remaining two nodes (see Figure 5.1). During the transmission of the data field, just after a bit has successfully been transmitted, the sender is affected by a permanent supply voltage failure (visualized by the "↯" symbol). From this point on, the sender transmits recessive bits only. Complete the empty columns in Figure 5.2 with the signal values that the three CAN nodes transmit in response to this event.

Hint: *The general form of a CAN error frame is visualized in Figure 5.1. Assume that throughout the considered time interval, none of the receivers has any data to transmit. Assume further that since the last hardware reset of the three nodes, no other errors have occurred.*

+1 p. for the remaining recessive bits of the sender.

+3 p. for the correct determination of both receiver levels.

+1 p. for the determination of the correct bus level.

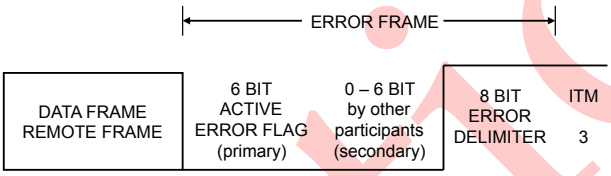


Figure 5.1: Error frame of the CAN protocol

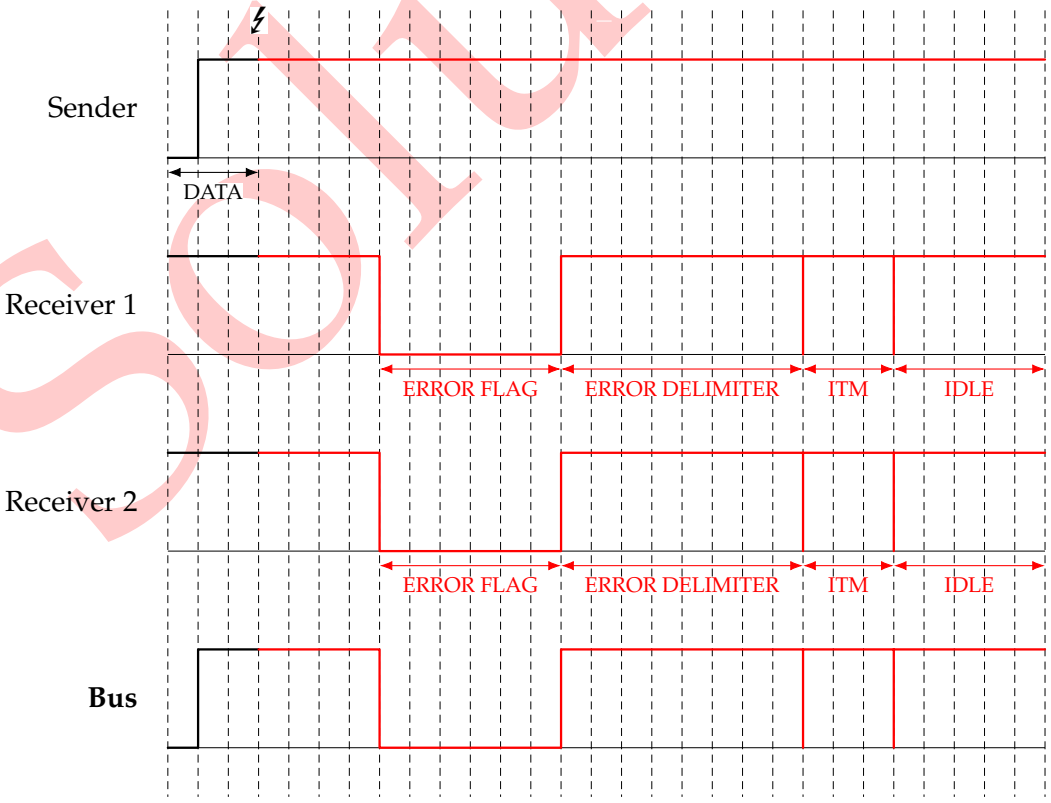


Figure 5.2: Signal sequence diagram of the CAN bus

B) How does the general concept of “error states” contribute to the robustness of a CAN network? Give a short explanation and name the error states that the protocol defines.

3

The error states ensure that malfunctioning participants are restricted or deactivated in order to protect the CAN bus itself. The protocol defines “error active”, “error passive”, and “bus off” as the three error states.

+1 p. for describing a plausible reason.

+2 p. for correctly naming the three modes.

C) Consider a CAN node that is connected to a CAN network with no further activated nodes. Initially, both its receive and its transmit error counter is zero. Suppose that this node begins to transmit an infinite stream of CAN messages, remains free from physical faults, and does not encounter any bit monitoring errors. Which error state will it eventually enter and retain? Justify your answer.

3

Initially, it is in the “error active” state. Due to the fact that no further CAN nodes are part of the network, it will receive no acknowledgments and eventually enter the “error passive” state. In this state, the lack of acknowledgments does not result in an increase of the transmit error counter value. Therefore, this is the error state that the considered CAN node retains.

+1 p. for the statement that the node will receive no acknowledgments.

+2 p. for recognizing that this keeps the node in the error passive state.

32

Task 6: Protocols

Task 6.1: FireWire Arbitration

The FireWire network shown below is given.

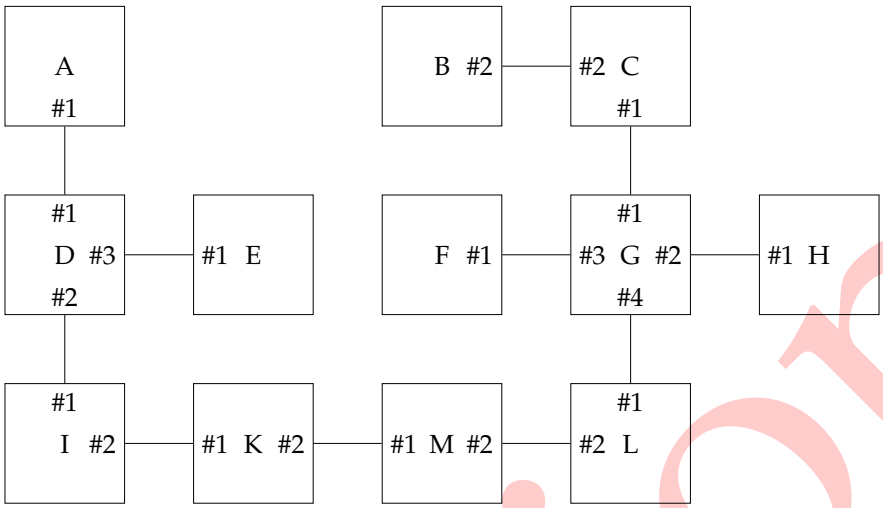


Figure 6.1: FireWire network

A normal FireWire bus cycle should be considered. For simplification, several assumptions should be taken into account:

- A list of nodes wanting to send is given.
- All nodes start requesting the bus at the same time.
- Processing of arbitration requests are done in zero time. There are no delays for propagation of the arbitration decision.
- If a node receives multiple bus requests, it will always forward the request that it receives from the port with the lowest number.

A) The nodes in Figure 6.1 are named using letters from A to M. What is the root of the FireWire network? The following nodes request access to the bus: **A, B, F, G, H, K, L**. Determine the order in which the nodes will be granted access to the bus.

6

root is node M, access order = K, A, L, G, B, H, F

2pt for root, 4pt for correct order
check order for wrong root

B) Which connection needs to be changed in Figure 6.1 in order to get node E as root. Hint: Only one connection needs to be removed and one connection needs to be inserted. You may mark the conecction in Fig. 6.1

2

remove connection between **node M and node L**
insert connection between **node E and node F**

2pt for correct

Task 6.2: FireWire Structures

6

A) Different FireWire structures were built during a student laboratory. During test phase you notice that not all FireWire systems are working. Please state if the FireWire systems given below are working correctly. Mark the roots, if the systems are correct. Give a reason, if the FireWire system is not working correctly.

1Pt each row
- when marked as wrong, reason is necessary.
- when marked as correct root is necessary.

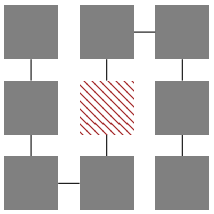
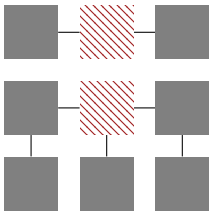
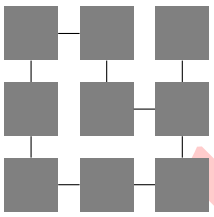
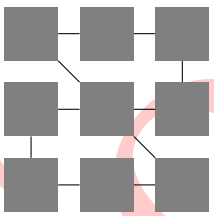
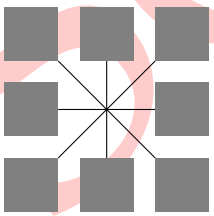
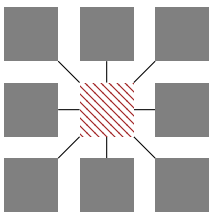
	Correct	Wrong	Reason
	x		
	x	x	wrong: two individual systems, correct two roots
		x	Rings are not allowed in FireWire
		x	Rings are not allowed in FireWire
		x	Stars are not allowed
	x		

Table 6.1: FireWire structures

Task 6.3: ITIV-Protocol

A customized protocol with multiple clients should be build for transmission of information with id and data.

A) The transmitted data-field can have any length between 2 and 64 bits. To determine the length of the data either an additional length-field or a delimiter can be used. What is the minimum additional worst case overhead when using an additional length-field? **2**

additional length field in frame. Needs $log_2(64-2) \equiv 6$ additional bits

2pt for length-field, -> 0pt if calculated with $log_2(64) \equiv 7$ bits

B) In the above task, consider when a delimiter is used. Consider a case where a delimiter of size 6 bits is used and another case where a delimiter of size 16 bits is used. Explain advantage and disadvantage of the different sized delimiters with respect to bitstuffing. **2**

Shorter delimiter can result in more bitstuffing. Longer delimiter can results in less bitstuffing but higher additional overhead.

+1 for each explanation. Other reasonable explanations possible.

C) The custom protocol should ensure data integrity. How can data integrity be checked on physical layer without adding additional bits or sending the data frame redundantly. **2**

Proper line coding needed, e.g. Mancheter, AMI, etc., which change at least once every clock cycle

2pt if correct

D) Besides of data integrity an error correction is necessary. Name a possible mechanism to correct faulty data without sending the data-field twice. **2**

error-correction code (ECC) or forward error correction (FEC): add redundant information to recover data
Minimal Hemming-Distance (e.g. Checksum) must be bigger or equal to 3 for one bit errors

2pt if correct

E) To read the data from the bus a clock recovery is neccessary. How can clock recovery be done without changing line code? **2**

Use preamble to synchronize the two clocks,
Bitstuffing/Block Codes (e.g. 4B/5B)

2pt if correct

F) In order to isolate the network and the components, the components should be capacitively coupled. Therefore a DC free conecction is necessary. Name two line codes to get an DC free transmission. **2**

Alternate Mark Inversion (AMI),
Manchester

1pt for each

G) Why can CSMA/CD not be used to transmit frames of 64 bit data from campus north to campus south (10 km) on a copper Gigabit line? What's the maximum allowed transmission bitrate to use this arbitration? **4**

The data to be send has to be long enough for the signal to travel **twice** the media during sending time.

$2 \cdot S_{max} = v \cdot t_{Frame}$
$2 \cdot 10km = 2/3 \cdot 3 \cdot 10^8 \cdot t_{Frame}$
$t_{Frame} = \frac{2 \cdot 10 \cdot 10^3 m}{2/3 \cdot 3 \cdot 10^8} = 1 \cdot 10^{-4} = 0,0001s = \frac{size_{Frame}}{bitrate}$
(if $2.5 \cdot 10^8$ is used then $t_{frame} = \frac{20}{25} \cdot 10^{-4} = 8 \cdot 10^{-5}$)

$bitrate = 64bit/0,0001s = 640 \cdot 10^3 bit/s = 640kbit/s$
(if $2.5 \cdot 10^8$ is used then $bitrate = 64bit/8 \cdot 10^{-5} bit/s = 800 \cdot 10^3 bit/s = 800kbit/s$)

2pt for correct answer reasoning
2pt for calculation
-1pt if travel time is not twice the distance
-1pt if only t_{Frame} is calculated
lecture defines $v = 2/3 \cdot c$
exercise defines $v = 2.5 \cdot 10^8$

H) How can a network made real time capable for all participants? **2**

An appropriate protocol and media access have to be chosen: **2pt for correct answer**
Examples: token passing at protocol level, Frequency division, time division
All access is controlled by one master
Use proper schedule for real time

Task 7: Routing

33

Task 7.1: NoCs

A) Name the three building blocks of a NoC and explain their basic function.

6

router switches paths and decides on the direction of the data
link/interconnect represents the physical communication channel
network interface is attaching processing elements to the network

alternatives : tile instead of network interface ; tile = processing unit

each 2 Point

B) Both NoCs and bus systems have their advantages and disadvantages. Compare both systems in terms of their scalability with increasing demand for bandwidth due to additional participants.

2

variable Bandwidth is provided by NoCs allowing it to be easily scalable meanwhile bus systems have a constant bandwidth not scaling with more participants.

2 Point

C) Describe and explain the two switching schemes circuit and packet switching.

4

circuit switching : messages are sent in their entirety using an pre-established path between sender and receiver.
packet switching : messages are partitioned into packets send consecutively and potentially using different paths in the network.

each 2 Points

D) Which switching approach is preferable in networks, where messages are sent rarely and with small payloads ? Explain the reasons for your choice.

2

packet switching, as circuit switching requires set up of the connection.
Alternative : circuit switching, more resource efficient since no message buffer required

2 Points

Task 7.2: Routing

A) Routing approaches are tightly coupled to a network's topology. Name and describe one algorithm that can be efficiently used for mesh topologies and one that is efficient for irregular topologies. Compare these algorithms in terms of their complexity.

6

Mesh topologies allow for usage of XY-Routing.
Irregular topologies require exploratory approaches, such as Dijkstra.
Alternative : Hot Potato, always use most cost-efficient port
These algorithms are typically more complex than for example XY-Routing.

2Pt Mesh routing 2Pt Irregular 2Pt for complexity comparison

B) Explain both static and dynamic routing algorithms. For each routing scheme describe a network in which the respective scheme is preferable.

6

Static (Deterministic) predefined paths
Preferable in robust networks that operate consistently under the same conditions
Dynamic (Adaptive) routing paths are calculated on the fly
Preferable in highly volatile networks with characteristics changing during runtime

1 Point for static and dynamic explanation 2 Points for each example

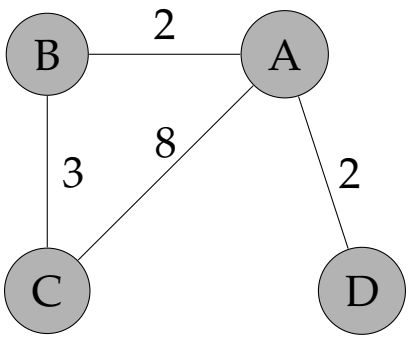


Figure 7.1: Given network topology

C) Figure 7.1 represents a network for which an optimal routing has to be found. The weights represent an abstract metric for traffic present at each connection. With node C as the starting point, calculate the paths with the lowest total traffic in the network by using Dijkstra's algorithm. For that write down the order in which nodes are visited in each bracket under the current step and fill out the given tables that encompass the shortest paths after each visitation of a node.

7

	step 1		step 2		step 3		step 4		step 5	
node	C		C		B		A		D	
vertex	trf.	pred.	trf.	pred.	trf.	pred.	trf.	pred.	trf.	pred.
A	∞	-	8	C	5	B	5	B	5	B
B	∞	-	3	C	3	C	3	C	3	C
C	∞	C	0	C	0	C	0	C	0	C
D	∞	-	∞	-	∞	-	7	A	7	A

Table 7.1: Dijkstra's algorithm

2 Points each step 2,3,4
1 Point for step 5 and correct nodes in the node row

Task 8: Network Topologies

30

Task 8.1: General Questions

A) Explain diameter of a network. What is the diameter of a 12x5 mesh network?

2

The Diameter of a network is the largest, minimal hop count over all pairs of nodes.
15

+1 for each answer

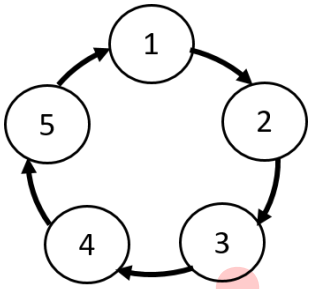


Figure 8.1: A five node unidirectional ring network

B) What is the diameter of a N node unidirectional Ring network? A 5 node unidirectional ring network is shown in Figure 8.1 as an example. Is such a topology suitable for safety critical applications? Explain your answer.

2

N-1
No. Because if one of the links fail, the node after it is not reachable by the other nodes. Communication is cut off.

+1 for N-1
+1 or reasonable explanation

C) Compute the Edge Connectivity and Diameter for 5x3 Torus, 15 node Star and 15 node Ring topologies. All links here are bidirectional. Use the table below.

6

+1 for correct answer

Topology	Edge Connectivity	Diameter
5x3 Torus	4	3
Star	1	2
Ring	2	7

Table 8.1: Topologies and Metrics

Task 8.2: 3D Topology

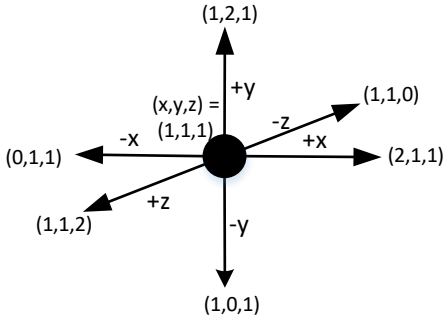


Figure 8.2: Node at (x,y,z) = (1,1,1)

A) Consider a 4x8x6 3D mesh topology for this task. There is a congestion present in the link from node (1,3,1) to node (1,2,1). Find the path from the source point (x,y,z) = (2,4,1) to the destination point (x,y,z) = (1,2,2) using the routing algorithm described below: **5**

Rule1 Try to first route in the X direction towards the destination. Then the Y direction, and then the Z direction.

Rule2 If the link chosen is congested, disregard it and choose among the remaining directions from the local position towards the destination, prioritising first X, then Y, then Z.

Rule3 In case none of the above rules is possible, choose among the remaining directions in the decreasing order of priority +x,+y,+z,-x,-y,-z. Use Figure 8.2 as a guide .Here it is possible for the packet to go away from the destination.

In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence. Mention which of the above mentioned rules you used at each step to go to the next node.

(2,4,1) (R1) -> (1,4,1) (R1) -> (1,3,1) (R2) -> (1,3,2) (R1) -> (1,2,2)

+1 pt per intermediate step (start and end point are optional and don't give extra points)
+1 pt for mentioning all rules correctly
+1 pt for a full solution with no errors

B) Another congestion has occured in the network along with the previous one. The new congestion is present in the link from (2,5,4) to (2,6,4). Find the path from the source point (2,3,4) to the destination point (2,7,4). In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence. Mention which rule you used at each step to go to the next node. What do you notice ? Explain your answer. **9**

(2,3,4)(R1) -> (2,4,4)(R1) -> (2,5,4) (R3) -> (3,5,4)(R1) -> (2,5,4) (R3)-> (3,5,4)

+1 pt per intermediate step of (2,4,4) -> (2,5,4) -> (3,5,4) -> (2,5,4) -> (3,5,4)
+2 pts if all the rules are mentioned correctly
-1 pt if one rule if incorrect
+1 pt if livelock is mentioned or if a reasonable explanation is provided. Example: loop,the packet is being forwarded forever
+1 pt for a full solution with no errors

C) Is the result of the above routing algorithm minimal? Explain your answer. **1**

No. Because it did not select the minimal route evertime due to congestion.

+1 pt for reasonable explanation

D) What is the diameter and edge connectivity of a 4x8x6 3D Mesh topology. **2**

Diameter = 3+7+5 = 15
Edge connectivity = 3

+2 pt for each correct explanation

E) Explain deadlock and livelock in a network. **2**

Deadlock : A situation where a link is blocked by one transmission that is waiting for the other transmission to finish is called a deadlock. Mutual blocking of links.
Livelock : Data is forwarded through a network without reaching its destination

+2 pt for each correct explanation

F) Name one motivation for using virtual channels in a NoC router. **1**

In larger networks, messages might have to wait for other messages to be transported. Link is blocked for circuit switching. Message buffer is blocked for packet switching

+1 pt for reasonable explanation

To solve this problem of bad link utilization, virtual channels can be used to share the physical link between multiple communications.
Multiplexing of physical links.

Additional sheet for task ☐ **:**